AMENDMENTS TO THE CLAIMS

15. (Previously Amended) A semiconductor chip having a substrate of a first conductivity type, the chip comprising:

a plurality of pads;

an electrostatic discharge (ESD) negative ring:

a plurality of ESD positive lines, the plurality of positive lines not being electrically connected to each other, none of the positive lines being directly connected to a pad;

a plurality of ESD switches connected to the ESD positive lines and the ESD negative ring so that each ESD switch is connected to a positive line and the ESD negative ring;

a plurality of first diodes connected to the pads so that each first diode is connected to a pad and the negative ring; and

a plurality of second diodes connected to the pads so that each second diode is connected to a pad and a positive line.

19. (Original) The chip of claim 15 wherein the ESD negative ring encircles the periphery of the chip.

38. (Previously Added) The chip of claim 19 wherein none of the plurality of positive lines encircles the periphery of the chip.

39. (Previously Added) The chip of claim 15 wherein a switch of the plurality of switches includes a transistor connected to a positive line and the negative ring.

40. (Previously Amended) A semiconductor chip having a substrate of a first conductivity type, the chip comprising:

a plurality of pads;

an electrostatic discharge (ESD) negative ring:

a plurality of ESD positive lines, the plurality of positive lines not being electrically connected to each other, none of the positive lines being directly connected to a pad;

a plurality f ESD switches connected to the ESD positive lines and the ESD negative ring s that each positiv line is connected to the negative ring via an ESD switch;

a plurality of first diodes connected to the pads so that each first diode is connected to a pad and the negative ring, a first diode of the plurality of first diodes including:

a plurality of first regions, the plurality of first regions being spaced apart from each other;

a second region, the plurality of first regions being formed in the second region, the plurality of first regions and the second region having opposite conductivity types, the second region having a dopant concentration; and

a third region formed in the second region, the third region being spaced apart from each first region, and formed between each adjacent pair of first regions, the third region having a dopant concentration that is higher than the dopant concentration of the second region; and

a plurality of second diodes connected to the pads so that each second diode is connected to a pad and a positive line.

41. (Previously Added) The semiconductor chip of claim 40 wherein the second region is formed in the substrate, the second region and the substrate having opposite conductivity types.

42. (Previously Added) The chip of claim 41 wherein the plurality of first regions have a dopant concentration that is higher than the dopant concentration of the substrate.

43. (Previously Added) The semiconductor chip of claim 40 and further comprising a fourth region, the second region being formed in the fourth region, the second region and the fourth region having a same conductivity type and different dopant concentrations, the fourth region being formed in the substrate, the fourth region and the substrate having opposite conductivity types.

44. (Previously Added) The chip of claim 43 wherein the plurality of first regions have a dopant concentration that is higher than the dopant concentration of the substrate.

45. (Previously Amended) The chip of claim 15 wherein the ESD positive lines are never directly connected to a steady voltage source.

46. (Previously Added) The chip of claim 45 wherein each second diode has an anode electrically connected to a pad.

47. (Previously Added) The chip of claim 46 wherein a positive line is connected to the negative ring via a plurality of ESD switches.

48. (Previously Added) The chip of claim 15 wherein each second diode has an anode electrically connected to a pad.

49. (Previously Added) The chip of claim 48 wherein a positive line is connected to the negative ring via a plurality of ESD switches.

50. (Previously Added) The chip of claim 15 wherein a positive line is connected to the negative ring via a plurality of ESD switches.

51. (Previously Amended) A semiconductor chip having a substrate of a first conductivity type, the chip comprising:

a plurality of pads;

an electrostatic discharge (ESD) negative ring:

a plurality of ESD positive lines, the plurality of positive lines not being electrically connected to each other;

a plurality of ESD switches connected to the ESD positive lines and the ESD negative ring so that each ESD switch is connected to a positive line and the ESD negative ring, a

switch f the plurality of ESD switches passing a current from a positive line to the negative ring when a voltag on the positive line rises at a first rate;

a plurality of first diodes connected to the pads so that each first diode is connected to a pad and the negative ring; and

a plurality of second diodes connected to the pads so that each second diode is connected to a pad and a positive line.

52. (Previously Amended) The chip of claim 51 wherein the switch blocks a current from flowing from the positive line to the negative ring when a voltage on the positive line rises at a second rate that is different from the first rate.

53. (Previously Amended) The chip of claim 51 wherein a second diode is forward biased when the voltage on the positive line rises at the second rate.

54. (Previously Added) The chip of claim 51 wherein none of the plurality of positive lines encircles the periphery of the chip.

55. (Previously Added) The chip of claim 51 wherein a positive line is connected to the negative ring via a plurality of ESD switches.

56. (Previously Amended) The chip of claim 51 wherein an ESD switch is directly connected to a positive line and the negative ring.

57. (Previously Amended) A semiconductor chip having a substrate of a first conductivity type, the chip comprising:

a plurality of pads;

an electrostatic discharge (ESD) negative ring:

a plurality of ESD positive lines, the plurality of positive lines not being electrically connected to each other, none of the positive lines being directly connected to a pad;

a plurality of ESD switches connected to th ESD positive lines and the ESD negative ring so that each ESD switch is connected to a positive line and the ESD negative ring;

a plurality of first diodes connected so that each first diode is connected between a pad and the negative ring; and

a plurality of second diodes connected so that each second diode is connected between a pad and a positive line.

58. (Currently Amended) ~~The semiconductor chip of claim 57 wherein~~ A semiconductor chip having a substrate of a first conductivity type, the chip comprising:

a plurality of pads;

an electrostatic discharge (ESD) negative ring;

a plurality of ESD positive lines, the plurality of positive lines not being electrically connected to each other, none of the positive lines being directly connected to a pad;

a plurality of ESD switches connected to the ESD positive lines and the ESD negative ring so that each ESD switch is connected to a positive line and the ESD negative ring;

a plurality of first diodes connected so that each first diode is connected between a pad and the negative ring, a first diode of the plurality of first diodes ~~comprises~~ comprising:

a plurality of first regions, the plurality of first regions being spaced apart from each other;

a second region, the plurality of first regions being formed in the second region, the plurality of first regions and the second region having opposite conductivity types, the second region having a dopant concentration; and

a third region formed in the second region, the third region being spaced apart from each first region, and formed between each adjacent pair of first regions, the third region having a dopant concentration that is higher than the dopant concentration of the second region; and

a plurality of second diodes connected so that each second diode is connected between a pad and a positive line.

59. (Previously Added) The semiconductor chip of claim 58 wherein the second region is f rmed in the substrate, the second region and the substrate having opposite conductivity types.

60. (Previously Amended) The semiconductor chip of claim 57 wherein an ESD switch is directly connected to a positive line and the negative ring.

61. (Previously Added) The semiconductor chip of claim 57 wherein none of the positive lines encircles the periphery of the chip.

62. (Previously Amended) A semiconductor chip having a substrate of a first conductivity type, the chip comprising:

a plurality of pads;

an electrostatic discharge (ESD) negative ring:

a plurality of ESD positive lines, the plurality of positive lines not being electrically connected to each other;

a plurality of ESD switches connected to the ESD positive lines and the ESD negative ring so that each ESD switch is connected to a positive line and the ESD negative ring, a switch of the plurality of ESD switches passing a current from a positive line to the negative ring when a voltage on the positive line rises at a first rate that is faster than a second rate;

a plurality of first diodes connected so that each first diode is connected between a pad and the negative ring; and

a plurality of second diodes connected so that each second diode is connected between a pad and a positive line.

63. (Currently Amended) ~~The semiconductor chip of claim 62 wherein~~ A semiconductor chip having a substrate of a first conductivity type, the chip comprising:

a plurality of pads;

an electrostatic discharge (ESD) negative ring:

a plurality of ESD positive lines, the plurality of positive lines not being electrically connected to each other;

a plurality of ESD switches connected to the ESD positive lines and the ESD negative ring so that each ESD switch is connected to a positive line and the ESD negative ring, a switch of the plurality of ESD switches passing a current from a positive line to the negative ring when a voltage on the positive line rises at a first rate that is faster than a second rate;

a plurality of first diodes connected so that each first diode is connected between a pad and the negative ring, a first diode of the plurality of first diodes ~~comprises~~ comprising:

a plurality of first regions, the plurality of first regions being spaced apart from each other;

a second region, the plurality of first regions being formed in the second region, the plurality of first regions and the second region having opposite conductivity types, the second region having a dopant concentration; and

a third region formed in the second region, the third region being spaced apart from each first region, and formed between each adjacent pair of first regions, the third region having a dopant concentration that is higher than the dopant concentration of the second region; and

a plurality of second diodes connected so that each second diode is connected between a pad and a positive line.

64. (Previously Added) The semiconductor chip of claim 63 wherein the second region is formed in the substrate, the second region and the substrate having opposite conductivity types.

65. (Previously Amended) The semiconductor chip of claim 62 wherein an ESD switch is directly connected to a positive line and the negative ring.

66. (Previously Added) The semiconductor chip of claim 62 wherein none of the positive lines encircles the periphery of the chip.

67. (Previously Added) A semiconductor chip having a substrate of a first conductivity type, the chip comprising:

a plurality of pads;

an electrostatic discharge (ESD) negative ring:

a plurality of ESD positive lines, the plurality of positive lines not being electrically connected to each other;

a plurality of ESD switches connected to the ESD positive lines and the ESD negative ring so that each positive line is connected to the negative ring via an ESD switch;

a plurality of first diodes connected to the pads so that each first diode is connected to a pad and the negative ring, a first diode of the plurality of first diodes comprising:

a plurality of first regions, the plurality of first regions being spaced apart from each other;

a second region, the plurality of first regions being formed in the second region, the plurality of first regions and the second region having opposite conductivity types, the second region having a dopant concentration; and

a third region formed in the second region, the third region being spaced apart from each first region, and formed between each adjacent pair of first regions, the third region having a dopant concentration that is higher than the dopant concentration of the second region; and

a plurality of second diodes connected to the pads so that only one second diode is connected between a pad and a positive line.

68. (Previously Added) A semiconductor chip having a substrate of a first conductivity type, the chip comprising:

a plurality of pads;

an electrostatic discharge (ESD) negative ring:

a plurality of ESD positive lines, the plurality of positive lines not being electrically connected to each other;

a plurality of ESD switches connected to the ESD positive lines and the ESD negative ring so that each positive line is connected to the negative ring via an ESD switch, a switch of

the plurality f ESD switches passing a current from a positive line to the negative ring when a voltage on the positive lin rises at a first rate;

a plurality of first diodes connected to the pads so that each first diode is connected to a pad and the negative ring, a first diode of the plurality of first diodes comprising:

a plurality of first regions, the plurality of first regions being spaced apart from each other;

a second region, the plurality of first regions being formed in the second region, the plurality of first regions and the second region having opposite conductivity types, the second region having a dopant concentration; and

a third region formed in the second region, the third region being spaced apart from each first region, and formed between each adjacent pair of first regions, the third region having a dopant concentration that is higher than the dopant concentration of the second region; and

a plurality of second diodes connected to the pads so that only one second diode is connected between each pad and each positive line.

69. (Previously Added) The chip of claim 15 wherein a second diode is directly connected to a pad and directly connected to a positive line.

70. (Previously Added) The chip of claim 57 wherein a second diode is directly connected to a pad and directly connected to a positive line.

71. (Previously Added) The chip of claim 51 wherein a second diode is directly connected to a pad and directly connected to a positive line.

72. (Previously Added) The chip of claim 62 wherein a second diode is directly connected to a pad and directly connected to a positive line.